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APPLICATION NO. FILING DATE		G DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,621	07/25/2006		Hubert Moriceau	(BIF 116044 US)	2319
7590 05/15/2007 Brinks Hofer			EXAM	EXAMINER	
Gilson & Lione PO Box 10395 Chicago, IL 60610			PATEL, REEMA		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/565,621	MORICEAU ET AL.
Office Action Summary	Examiner	Art Unit
	Reema Patel	2812
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	e correspondence address
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be will apply and will expire SIX (6) MONTHS from cause the application to become ABANDO	ON. timely filed om the mailing date of this communication. NED (35 U.S.C. § 133).
Status		
3) Since this application is in condition for allowar	action is non-final. nce except for formal matters, p	
closed in accordance with the practice under E	х рапе Quayle, 1935 С.D. 11,	453 O.G. 213.
Disposition of Claims		
 4) Claim(s) 1-40 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1-40 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or 	vn from consideration.	
Application Papers		
 9) The specification is objected to by the Examiner 10) The drawing(s) filed on 19 January 2006 is/are: Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11) The oath or declaration is objected to by the Examiner 	a) \square accepted or b) \square objected or by accepted in abeyance. So in is required if the drawing(s) is \square	See 37 CFR 1.85(a). Objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the prior application from the International Bureau * See the attached detailed Office action for a list of 	s have been received. s have been received in Applicative documents have been received in PCT Rule 17.2(a)).	ation No ved in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 1/19/06,3/5/07,3/22/07.	4) Interview Summa Paper No(s)/Mail 5) Notice of Informa 6) Other:	

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DETAILED ACTION

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Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statements (IDS) were submitted on 1/19/06, 3/05/07, and 3/22/07. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 4. Claims 1-2, 26-28, 31-38, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (U.S. 6,156,215).
- 5. Regarding claim 1, Shimada et al. discloses the following claimed elements:
 - A method of fabricating a stacked structure, comprising:

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Selecting a first plate (1, Fig. 1A) and a second plate (8, Fig. 1D) such that
a portion of at least one of the first and second plates has a structured
surface (Fig. 1A);

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- Producing a sacrificial layer (4, Fig. 1A) on at least a portion of the structured surface of the first plate or the structured surface of the second plate;
- Bonding the two plates together (Fig. 1E).
- 6. Regarding claim 2, Shimada et al. discloses structuring at least a portion of the first plate and the second plate (Fig. 1A, 1D).
- 7. Regarding claim 26, Shimada et al. discloses a stacked structure fabricated by the method of claim 1 (Fig. 1A-1E).
- 8. Regarding claim 27, Shimada et al. discloses a stacked structure comprising a sacrificial layer between a first substrate and a second substrate wherein at least a portion of at least one of the first or second substrates comprises a structured surface (Fig. 1A-1E; col 3, lines 18-24).
- 9. Regarding claim 28, Shimada et al. discloses that the structured surface comprises a surface having predetermined physical-chemical properties (col 3, lines 18-24).
- 10. Regarding claim 31, Shimada et al. discloses that at least one of the first or second substrates has a surface layer (col 3, lines 41-44).
- 11. Regarding claim 32, Shimada et al. discloses that the surface layer comprises a monocrystalline surface layer (col 6, lines 37-41).

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12. Regarding claim 33, Shimada et al. discloses that the surface layer comprises silicon (col 6, lines 37-41).

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- 13. Regarding claim 34, Shimada et al. discloses that the surface layer comprises a material having predetermined physical-chemical properties (col 6, lines 37-41).
- 14. Regarding claim 35, Shimada et al. discloses that the surface layer comprises silicon nitride (col 6, lines 37-41).
- 15. Regarding claim 36, Shimada et al. discloses that a major portion of at least one of the first or second substrates comprises a semiconductor material (col 6, lines 1-4).
- 16. Regarding claim 37, Shimada et al. discloses that the major portion comprises silicon (col 6, lines 1-4).
- 17. Regarding claim 38, Shimada et al. discloses the sacrificial layer comprises silicon oxide (col 6, lines 16-21).
- 18. Regarding claim 40, Shimada et al. discloses wherein at least one of the first or second substrates comprises a thin layer (Fig. 1A; col 3, lines 18-25).
- 19. Claims 1, 3-8, 12-13, 16-18, 21-24, 26-27, and 29-30 rejected under 35 U.S.C. 102(e) as being anticipated by Lei et al. (2005/0042842 A1).
- 20. Regarding claim 1, Lei et al. discloses the following claimed elements:
 - A method of fabricating a stacked structure, comprising:
 - Selecting a first plate and a second plate such that a portion of at least one of the first and second plates has a structured surface ([0040]-[0041]);

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 Producing a sacrificial layer on at least a portion of the structured surface of the first plate or the structured surface of the second plate ([0042]);

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- Bonding the two plates together ([0046]).
- 21. Regarding claim 3, Lei et al. discloses wherein selecting a first plate and a second plate comprises selecting plates having predetermined physical-chemical properties ([0040]).
- 22. Regarding claim 4, Lei et al. discloses that the roughness of the surface is greater than a predetermined threshold ([0041]).
- 23. Regarding claim 5, Lei et al. discloses that the predetermined threshold is approximately 0.2 nm root-mean-square (RMS) ([0041]).
- 24. Regarding claim 6, Lei et al. discloses that at least one of the plates includes a surface layer ([0045]).
- 25. Regarding claim 7, Lei et al. discloses that the surface layer comprises a monocrystalline surface layer ([0042], [0045]).
- 26. Regarding claim 8, Lei et al. discloses that the surface layer comprises silicon ([0042], [0045]).
- 27. Regarding claim 12, Lei et al. discloses smoothing at least one of a free surface of the sacrificial layer or a free surface of at least one of the plates because the bonding ([0031]).
- 28. Regarding claim 13, Lei et al. discloses smoothing the free surface of the sacrificial layer and the free surface of at least one of the plates before the bonding ([0031]).

- 29. Regarding claim 16, Lei et al. discloses that the bonding is assisted by at least one of a mechanical means, a plasma treatment, or a thermal treatment ([0047]).
- 30. Regarding claim 17, Lei et al. discloses applying a selected atmosphere before bonding ([0031]).
- 31. Regarding claim 18, Lei et al. discloses wherein assisting further comprises applying a selected atmosphere during bonding ([0030]).
- 32. Regarding claim 21, Lei et al. discloses thinning at least one of the first or second plates after bonding ([0047]).
- 33. Regarding claim 22, Lei et al. discloses a major portion of at least one of the first or second plates comprises a semiconductor material ([0040]).
- 34. Regarding claim 23, Lei et al. discloses the major portion comprises silicon ([0040]).
- 35. Regarding claim 24, Lei et al. discloses the sacrificial layer comprises silicon oxide ([0042]).
- 36. Regarding claim 26, Lei et al. discloses a stacked structure fabricated by the method of claim 1 (Fig. 2A-2F).
- 37. Regarding claim 27, Lei et al. discloses a stacked structure comprising a sacrificial layer between a first substrate and a second substrate wherein at least a portion of at least one of the first or second substrates comprises a structured surface (Fig. 2A-2F).
- 38. Regarding claim 29, Lei et al. discloses that the structured surface has a roughness greater than a predetermined threshold ([0041]).

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39. Regarding claim 30, Lei et al. discloses that the predetermined threshold is approximately 0.2 nm ([0041]).

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Claim Rejections - 35 USC § 103

- 40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 41. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei et al. (2005/0042842 A1) as applied to claim 1 above, and further in view of Yee et al. ("Polysilicon surface-modification technique to reduce sticking of microstructures").
- 42. Regarding claim 9, Lei et al. discloses a surface layer but does not disclose that it is structured. However, according to Yee et al., it is desirable to structure the surface of a layer so as to be able to eliminate undesirable sticking between microstructures (page 145, "Introduction"). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lei et al. with structuring the surface layer, as taught by Yee et al., so as to be able to eliminate sticking between an insulating layer and freed wafer surface during an SOI wafer fabrication process.
- 43. Regarding claims 10-11, Lei et al. discloses a surface layer of silicon nitride. which has predetermined physical-chemical properties ([0042], [0045]).

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- 44. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lei et al. (2005/0042842 A1) as applied to claim 1 above, and further in view of Maleville et al. (U.S. 6,429,094 B1).
- 45. Regarding claim 14, Lei et al. discloses that the substrates are bonded together but does not disclose that such a procedure is done via molecular bonding. However, Maleville et al. discloses the use of molecular bonding in forming an SOI-type substrate (col 3, lines 51-54) since it allows for a strong bond between two substrates and enables un-bonding of the substrates along the bonding interface (col 3, lines 38-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lei et al. with bonding by molecular bonding, as taught by Maleville et al., so as to achieve a strong bond between two substrates while also enabling un-bonding of the substrates along the bonding interface.
- 46. Claims 15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei et al. (2005/0042842 A1) as applied to claim 1, above and further in view of Hosoma et al. (U.S. 6,198,159 B1).
- 47. Regarding claims 15 and 25, Lei et al. discloses a sacrificial layer but does not disclose that it comprises a polymer ([0042]). However, Hosoma et al. discloses using a polymer as a sacrificial bonding layer (col 1, lines 34-41) so that bonding between wafers can be done under relatively mild conditions with uniformity (col 1, lines 29-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lei et al. with using a sacrificial

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bonding agent of a polymer sacrificial layer, as taught by Hosoma et al., so as to be able to bond two wafers under relatively mild conditions with uniformity.

- 48. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei et al. (2005/0042842 A1) as applied to claim 16 above, and further in view of Haberger et al. (U.S. 6,417,075 B1).
- 49. Regarding claims 19-20, Lei et al. discloses bonding in the closed atmosphere of a bonding chamber ([0030]) but does not disclose exposing the wafers to an open air environment before or during bonding. However, Haberger et al. discloses exposing wafers to an open air environment so as to form a natural oxide layer which serves as a bonding area (col 4, lines 61-64). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lei et al. with exposing the wafers before and during bonding to an open air environment, as taught by Haberger et al., so as to form a natural oxide on the wafer which serves as the bonding area.
- 50. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. 6,156,215) as applied to claim 27 above, and further in view of Hosoma et al. (U.S. 6,198,159 B1).
- 51. Regarding claim 39, Shimada et al. discloses a sacrificial layer but does not disclose that it comprises a polymer (col 6, lines 16-21). However, Hosoma et al. discloses using a polymer as a sacrificial bonding layer (col 1, lines 34-41) so that bonding between wafers can be done under relatively mild conditions with uniformity

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(col 1, lines 29-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lei et al. with using a sacrificial polymer layer, as taught by Hosoma et al., so as to be able to bond two wafers under relatively mild conditions with uniformity.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aspar et al. (2004/0222500 A1), Aspar et al. (2003/0077885 A1), Moriceau et al. (U.S. 6,974,759 B2), and Ghyselen et al. (2005/0112845 A1) disclose methods of forming stacked structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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RSP 5/14/07

SCOTT B. GEYER PRIMARY EXAMINER

NP.M 5/14/07